# The chiprack project – a report on progress

M. Anstey, Luton, D. Holburn, D. Jordan und C. Hawkins, Cambridge

# Das „Chiprack"-Projekt – Fortschrittsbericht

## INTRODUCTION

This paper is divided into three sections. The first part covers elements of the background to the 'Chiprack' project. The second section reports on a recently completed SMART study carried out to assess the feasibility of using 'Chiprack' techniques to build an industry standard Personal Computer (PC) system. Finally the progress to date is summarised and some conclusions are drawn.

The authors would like to acknowledge the assistance of a Department of Trade and Industry SMART award (Small Firms Merit Award for Research and Technology) which enabled the PC feasibility study to take place.

## BACKGROUND

The Chiprack project began some eight years ago with a project brief to design an interconnection system which would facilitate automated assembly and would anticipate the outcome of established trends within the semiconductor industry[1].
Six major trends were identified:

1) Resolution of sub-assemblies into single VLSI components.
Even at that time (1985/6) whole boards of discrete circuitry were being reduced to single VLSI circuits. This trend has continued relentlessly and we now have PC motherboards on a single chip, single chip graphics controllers, single chip modems, single chip disk controllers - in fact most major functions of computer systems are now available as single chip solutions.

2) Increasing use of custom and semi-custom silicon.
A second trend was towards products that would consist of relatively few 'standard' VLSI parts, coupled by one or more custom parts. Several small computer systems consisting of a handful of VLSI components coupled by a large gate array had already been marketed. Gate arrays are now a standard feature of many designs. More importantly not only are they being used to mop up the discrete logic within a design but they are also being used to mop up sections of the interconnection network that used to be implemented on the printed circuit board.

3) Increasing production of 'families' of circuits.
It was anticipated that semiconductor manufacturers would increasingly design VLSI products with direct interconnection and use with other members of the 'family' in mind. Again this trend has continued to the extent that many of the semi-conductor manufacturers will now provide full schematics which show complete products formed by direct connection of small numbers of their VLSI circuits.

4) Proportional rise in interconnection and assembly costs would force adoption of automated assembly techniques.
It was anticipated that as the cost of integrated circuitry fell the relative cost of interconnection and assembly would become proportionally higher. Some companies would adopt automated assembly techniques and this would force the hand of the others. The use of expensive software controlled pick and place machinery has now become essential in order to competitively produce electronic products in any significant volumes.

5) Ascendency of low power technology.
It was anticipated that technologies offering lower power consumption would increasingly find favour in order to minimise heat dissipation (and power consumption) in mains powered devices, and to permit long support times in battery powered devices.

6) Demand for increased packing density.
Electronic products were, and are still, required to be ever smaller and more compact. Computer systems manufacturers, in particular, seek ever increasing amounts of processing power to be packed into smaller units.

There were 4 conclusions from this examination of trends.

1) Many products could be seen as being reduced to a small number of standard VLSI parts coupled together by one or more custom circuits.

2) The function of the custom circuit(s) would be not only to mop up the discrete logic within a system, but also to incorporate large sections of the interconnection needed to link the VLSI parts together. Programmable logic arrays would increasingly permit both logic and interconnect to be re-arranged under software control.

3) The variable geography of the printed circuit board determined the use of expensive software controlled pick and place machines to place components on the surface of the board. Once interconnect had been moved into custom circuits much simpler, faster, and vastly cheaper methods of automated assembly could be considered.

4) Interconnection systems design should anticipate demand for high packing densities and the use of lower power consumption circuitry.

A number of different interconnection systems were devised with these conclusions in mind, in an effort to optimise ease of automated assembly. Some were prototyped, but only one was considered to hold enough potential for further investigation. This interconnection system was called 'Chiprack'

## THE CHIPRACK INTERCONNECTION SYSTEM

The Chiprack interconnection system consists of two types of structure 'Carriers' and ' Connectors'.

### CARRIERS (see Fig 1)

Carriers are essentially leadless chip carriers (although they may also be Multi Chip Modules or small surface mount assemblies). They have contact pads on both upper and lower surface of the carrier. These pads are not through connected, although they can be, if required. The package is of such a shape and form to be

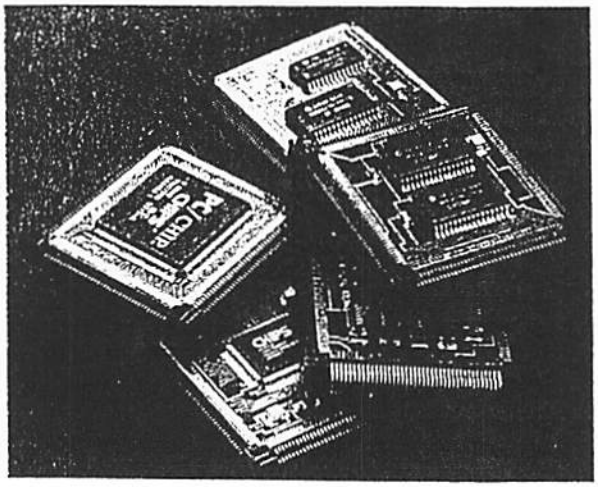

Figure 1. Carriers

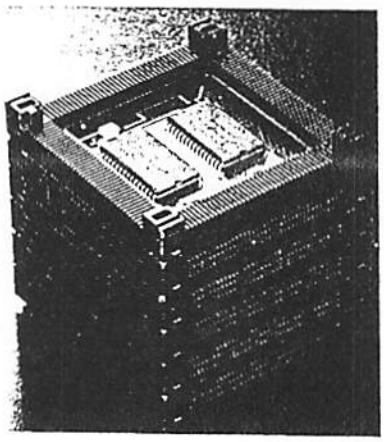

Figure 2. Connectors.

supplied to an assembling machine by an automated feed and therefore has to be robust enough to withstand mechanical handling and rapid travel during movement and orientation. The fine leaded style of carrier was rejected because of the danger of damage or distortion to the leads.

### CONNECTORS (see Fig 2)

The Connectors are stacking connectors which latch together by means of a small latch at each corner. Latches can be released by depressing the small button at each corner. Their basic function is to stack and interconnect a small number of carriers into a working product. The connectors have been designed to play a complex role and they perform several different functions.

1) The Connectors hold the Carriers in precise registration within the connector and ensure contacts and pads match up for connection or soldering purposes.

2) The Connector contacts provide connection only between the bottom row of contacts on one Carrier to the top row of contacts on an adjacent Carrier. It is most important to appreciate that they do NOT implement a bus through a stack.

3) The Connector contacts provide a heat path from the inside of a stack to the outside, and configure the outside to look and behave like a convoluted heat sink. The Connectors space Carriers one from another and ventilation of heat from both sides of each carrier is enabled.

4) The Connector contacts bring signals to the outside of the stack and provide easy access to all the signals as they pass from one circuit to another.

5) The Connectors can function as an edge connector socket for both external or internal connection purposes.

6) The Connectors surround and protect the Carriers, and facilitate encapsulation or shielding.

## SIGNAL PATHS IN CHIPRACK SYSTEMS

Electronic products are constructed by simply latching the Carriers and the Connectors into a small stack. Signals and power can be bussed through the stack (see Fig 3). Alternatively the intersection of each carrier in the stack presents the opportunity to re-organise the pattern of signals at that intersection. The interconnecting bus can be re-configured in hardware, or by software, at the intersection of each Carrier. Fig 4 shows a typical computer system with CPU (a) with local memory bus signals x, y, z . The patterning of these signals can be presented to pads on the underside of the Carrier holding memory array (b). These signals are configured and distributed to the memory array via tracking on the CPU Carrier (hardware reconfiguration). Alternatively Fig 5 shows CPU (a) and

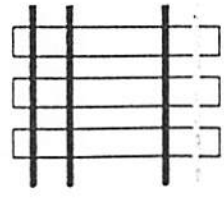

Figure 3.
Signals run as through bus.

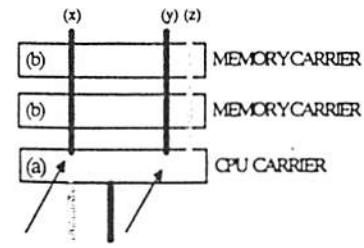


Figure 4.
Signals are moved into place by tracking on CPU carrier.

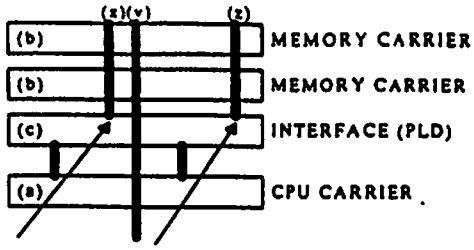


Figure 5. Signals are moved into place by programmable logic device (c) implementing the memory interface.

memory array (b) connected by memory interface, implemented by a Programmable Logic Device, (c). In either case if the memory requires changing or upgrading the patterning of signals can be re-configured to suit the new type of memory. In Fig 5 re-configuration would be by software re-configuration of the memory interface (c).

## SYSTEM FEATURES

A number of small experimental computer systems [2] were constructed to demonstrate the feasibility of real electronic systems being constructed in this way. These systems exhibited a number of interesting characteristics.

1) Carriers and connectors could be very rapidly assembled into working systems. Hand assembly rates of 2-3 systems per minute using minimal aids and jigs were possible. The nature of the assembly operation( stacking of Carriers and Connectors and then compressing them into working systems) could be carried out by a hard tooled machine costing a fraction of the cost of a software controlled pick and place machine.

2) The highly modular approach meant that systems could be designed as a series of modules or large VLSI chips, tested as a series of modules and could be altered, re-configured, repaired and extended in modular fashion. In these experimental computer systems the CPU could be taken out and upgraded when a new version appeared. Memory blocks could be added, memory types changed or substituted. I/O sub-systems could be added, changed or upgraded to suit particular requirements. The nearest analogy is that of a large electronic 'Lego' with large silicon blocks that can rapidly and flexibly be build into a wide range of electronic products.

3) Test and repair of systems is simplified. All the Carriers have a constant 'footprint' in common with the assembled working system for ease of attachment to test instruments. Malfunctioning systems are easily taken apart for replacement of faulty Carriers.

4) Systems were compact, robust and reliable. Volume reductions of over 70% on equivalent PTH board systems were typical. The connectors formed a rigid cage around the electronics, easy to encapsulate or shield, and reliable over a full range of shock and vibrational testing. The early experimental 68070 systems have now been working for over five years without problem.

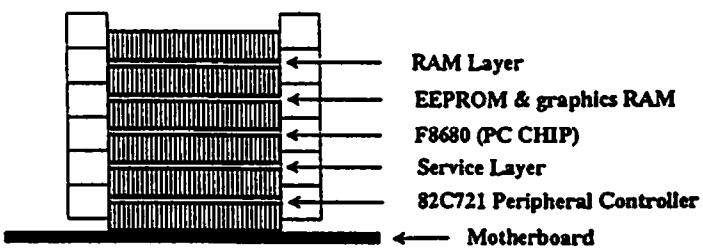


Figure 6. Diagram of experimental PC system.

## EXPERIMENTAL CHIPRACK PC SYSTEM FOR EMBEDDED APPLICATION

The second section of this paper reports on a recent study carried out to assess the feasibility of building an industry standard Personal Computer (PC) system by using Chiprack techniques. It was considered that such a system, if it could be made low cost, compact, robust and energy efficient could have a wide range of industrial and domestic applications. It could, for example, be embedded into instrumentation, vending machines, point of sale terminals and many types of control system. It was also considered that the silicon technology developed for the PC industry should be particularly suitable for the experimental Chiprack techniques. Over 110 million PCs have been sold worldwide and as a result the hardware base has probably evolved more rapidly than for any other electronic product. Single chip solutions have been generated for most PC functions and sub-systems. Single chip graphics controllers, single chip floppy and hard disk controllers, PC motherboards on a single chip all provide examples.

## THE EXPERIMENTAL PC SYSTEM (Fig 6)

The experimental PC system consists of a number of component Carriers and Connectors, which when stacked together, form a compact PC system.

The PC system is based around the Chips and Technologies F8680 PC/CHIP. This is a highly integrated 8086 compatible processor that provides all the functionality of a PC motherboard, including memory management, keyboard controller and an XT bus controller. In addition the F8680 also has a UART, an LCD graphics controller and support for PCMCIA memory cards. All these functions have been integrated onto a single VLSI chip.

The Carriers in the experimental system are:

1. Processor Carrier - This Carrier consists of the 160 pin surface mount package of the F8680 processor mounted onto a chiprack carrier. Certain of the signals from the F8680 pass up the stack to the memory array, some signals pass down to the Input/Output (I/O) section at the base, and others are routed throughout the whole system.

2. Service Carrier - The service Carrier sits below the processor . Its function is to provide the system clocks for the processor and a reset on power up signal. The carrier consists of a number of surface mount crystals, surface mount logic I.C.s and surface mount discretes. Since the experimental system was constructed one of

the semiconductor manufacturers has implemented all the system clocks required for this computer into one component. The modular approach adopted in this design means that upgrading simply involves the removal of this Carrier and replacement with the single component solution.

3. ROM and Graphics RAM Carrier - This Carrier is positioned above the processor Carrier. There are two surface mount I.C.s mounted on this Carrier. The first is a 128K byte electrically erasable memory (EEROM) containing the low level PC operating system (BIOS). There is also space free for application software or for ROM based DOS. The second I.C. is a 32K byte RAM to provide the video memory for the graphics controller of the F8680. A local bus is implemented between the F8680 and the video memory (i.e. the bus only runs between the F8680 Carrier and the video memory Carrier above).

4. RAM Carrier - On top of the ROM Carrier, there are one or more RAM Carriers providing the system memory. Two types of RAM Carrier have been produced. The first is a static RAM Carrier holding two 128K by 8 bit surface mount static RAM chips providing 256K bytes of memory. The second memory carrier is a dynamic RAM carrier containing two 512K by 8 bit dynamic RAM chips providing 1M byte of memory. Each memory carrier is identical and the memory selects for the RAM carriers are arranged in such a way that memory carriers are automatically configured as additional carriers are added (see Fig 7). This makes use of the unique inteconnection possibilities that Chiprack provides.

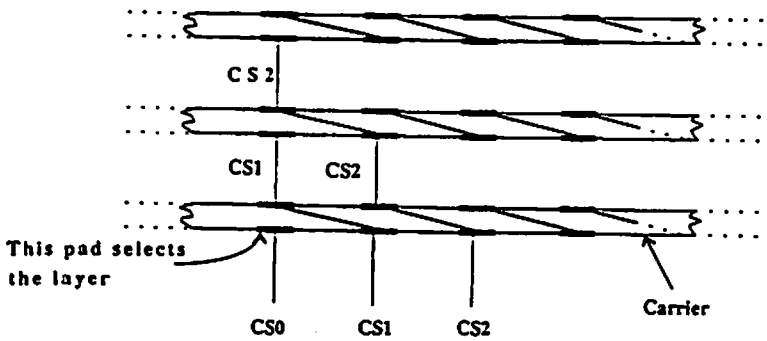


Figure 7.
Identical memory carriers route chip selects.

Memory types, static or dynamic, may be mixed but usually the system memory will consist of only one type. The memory type used is configured in the BIOS and the size of memory is automatically detected and tested on power up. The RAM carrier is a good example of the modularity of these stacked systems. It permits the type and size of memory to be chosen to suit any individual application simply by adding the required number and type of RAM carriers.

5. Multi I/O carrier - This carrier is an optional carrier. It supports all the standard I/O found in a PC system by providing a parallel port, two serial ports, a floppy disk controller and an IDE hard disk controller. It consists of a 100 pin surface mount I/O chip . For many applications the facilities provided by the four carriers already described would be sufficient however if more extensive I/O facilities are required that this carrier can be fitted onto the base of the stack.

The PC system is mounted on to a motherboard to provide connections between the peripherals and the tower. The present motherboard is intended for development purposes and provides standard connectors for a monitor, keyboard, power, parallel port, two serial ports, floppy disk, hard disk, and PCMCIA port. It also provides an expansion slot and a connection for a LCD display. Its physical size is set by the size of these standard connectors. For many applications this motherboard would not be required and any I/O connections would be taken directly from the stack.

## SUMMARY OF PROGRESS AND CONCLUSIONS

The experimental PC system behaves exactly like a standard PC. It will connect to a full range of PC compatible hardware as well as running standard PC software such as MS DOS and Windows, and yet all the solid state electronics is packed into a modular block some 55 ccm in volume. Carriers can be added, upgraded, repaired and re-designed all in modular fashion. As Carriers are added or modified the interconnecting bus can be re-configured at the point of interersection of any of the Carriers in order to meet the requirements of the additional resources. There are no heat or performance problems with the system running at 14MHz. Further experimental systems, using other processors running at 40-100MHz are planned which will take advantage of the short, regular interconnections between carriers. A controlled impedance contact to meet these performance targets is under investigation.

There are three general propositions suggested by the project: They are deliberately presented as contentious points for discussion.

1. The project has demonstrated an approach to modularity at the individual VLSI circuit level. It is proposed that this will become an increasing requirement with growing complexity of individual VLSI. At one time modularity was required at the level of circuit boards slotting into a backplane. Now those circuit boards have been integrated onto single chips the modularity is required at this new level - the single VLSI circuit.

2. Interconnect will increasingly move onto silicon. Commodity VLSI will be designed with direct interconnection in mind, and programmable parts will increasingly implement not only logic but also interconnect. As interconnect moves onto silicon the remainder of the interconnect in a system (i.e. the interconnect not on

silicon) can be implemented by connections which are simpler, more regular, and more suited to automated assembly. The Chiprack project has demonstrated that such connections can be implemented in a way which then permits rapid assembly by simple stacking, which can be carried out by a low cost hard tooled machine.

3. As interconnect moves onto silicon it will increasingly come under software control. This will happen not only in programmable logic devices but also as a result of usage of new VLSI parts dedicated entirely to programmable interconnect (some are already being marketed). This in turn will mean that interconnection systems will move away from fixed bus systems to re-definable bus architectures. The resources within an electronic system will start to determine the type and nature of the bus that is required to interconnect them. Addition of new resources may determine software re-configuration of the interconnecting bus. It is even possible to envisage systems where, under software control, local buses are established for the duration of particular operations.

## References


1) Anstey, M.: 'A Three Dimensional Interconnection System'. Electronic Engineering, March 1985.

2) Anstey, M.: 'Partitioning Electronic Circuits - A Key to Automated Assembly? The Chiprack Project'. International Conference on High Performance Electronic Packaging - London, November 1990, IEE/Welding Institute.


# On the extension of microbonding technology


S. Nakata, Osaka


# Erweiterte Anwendungen der Verbindungstechniken


Several problems and its backgrounds on the micro-bonding technology as the key one in the packaging technology are shown based on our researches.

As one of the fundamental problems, the interface temperature measurement and in-process control of the bond quality are shown on laser microbonding and hot tip microbonding process and its application to in-process control of the micro-bond.

Next, as one of future microbonding technology for more fine lead, microbonding process with active inserted-metal films of low melting point have been researched and discussed with its reliability.

Finally, newly developed automatic inspection system of the micro-bonds by infrared thermal image with laser irradiation have been shown with some applications to the detecting the micro-defects of the TAB bonds.


## 1 Introduction

The microbonding process is generally defined at the term for the bonding process where the work is too small to neglect the influence of the physical and chemical quantities which is incidental to the bonding on bondability and reliability.[1)]

As the fundamental and important problems in microbonding technology from the viewpoint of microbonding process to assure the quality of the micro-bond, interface temperature of the bond in bonding process and its application to the in-process control of the micro-bond quality, new developed bonding process with active inserted-metal film with low melting point, and furthermore, the inspection system of the TAB bond are shown and discussed, based on our researches.